

IN THE CLAIMS

1 1 – 9. (canceled).

1 10. (currently amended) ~~The integrated circuit chip package of claim 9~~ An integrated
2 circuit chip package comprising:
3 a metal substrate core;
4 the metal substrate core having at least two electrically isolated regions;
5 wherein at least one of the electrically isolated regions of the metal substrate core
6 is coupled with a digital ground of an integrated circuit chip, wherein input and output
7 signals of the integrated circuit chip are routed through the electrically isolated region of
8 the metal substrate core that is coupled with the digital ground of the integrated circuit
9 chip, and wherein at least one ~~other~~ of the electrically isolated regions of the metal
10 substrate core is coupled with an operating voltage rail of the integrated circuit chip.

1 11. (currently amended) The integrated circuit chip package of claim 9 10, wherein at
2 least one ~~other~~ of the electrically isolated regions of the metal substrate core is coupled
3 with an analog ground of the integrated circuit chip

1 12. (canceled)

1 13. (currently amended) ~~The integrated circuit chip package of claim 12~~ An
2 integrated circuit chip package comprising:

3 a metal substrate core;
4 the metal substrate core having at least three electrically isolated regions;
5 wherein at least one of the electrically isolated regions of the metal substrate core
6 is coupled with a digital ground of an integrated circuit chip and through this region input
7 and output signals are routed, and wherein at least one ~~other~~ of the electrically isolated
8 regions of the metal substrate core is coupled with an operating voltage rail of the
9 integrated circuit chip.

1 14. (currently amended) The integrated circuit chip package of claim ~~12~~ 13, wherein
2 at least one ~~other~~ of the electrically isolated regions of the metal substrate core is coupled
3 with an analog ground of the integrated circuit chip.

1 15 – 20. (canceled).